ficial pattern may be formed on the hard mask layer. The third sacrificial pattern may have an etching selectivity with respect to the hard mask layer. A fourth sacrificial pattern may be formed on the third sacrificial pattern. The fourth sacrificial pattern may have an etching selectivity with respect to the third sacrificial pattern.

[0015] In example embodiments, when the first spacer is formed, the second sacrificial pattern may be removed.

[0016] In example embodiments, the first spacer may be formed on a sidewall of the first sacrificial pattern, and the second spacer may be formed on sidewalls of the third and fourth sacrificial patterns.

[0017] In example embodiments, when the first preliminary mask pattern structure is removed, the first sacrificial pattern may be removed.

[0018] In example embodiments, when the second mask pattern structure is formed, the fourth sacrificial pattern may be removed.

[0019] In example embodiments, when the second pattern structure is formed, the third sacrificial pattern may be removed.

[0020] In example embodiments, two first mask pattern structures may be formed using each of one first preliminary mask pattern structure and one second preliminary mask pattern structure.

[0021] In example embodiments, the third and fourth widths may be equal or substantially equal to the first and second widths, respectively.

[0022] According to example embodiments, there is provided a method of forming patterns of a semiconductor device. In the method, first hard mask layer may be formed on an etch target layer, the etch target layer having first and second regions, and the second hard mask layer may be formed on the first hard mask layer. A first preliminary mask pattern and a first spacer may be formed on the second hard mask layer in the first region. The first spacer may be on a sidewall of the first preliminary mask pattern. Second and third preliminary mask patterns may be formed on the second hard mask layer on the second region. The second preliminary mask pattern may have an upper surface substantially coplanar with an upper surface of the first preliminary mask pattern, the third preliminary mask pattern formed on the first region, and the third preliminary mask pattern may have an etching selectivity with respect to the second hard mask layer. Second and third spacers may be formed on sidewalls of the second and third preliminary mask patterns. The first preliminary mask pattern may be removed. The second hard mask layer may be partially removed using the first and second spacers and the second and third preliminary mask patterns as an etching mask to form first and second mask pattern structures, the first mask pattern structure formed on the first region and having a first width, the second mask pattern formed on the second region and having a second width. The second width may be greater than the first width. Fourth and fifth spacers may be formed on sidewalls of the first and second mask pattern structures. The first hard mask layer may be partially removed using the fourth and fifth spacers and the first and second mask pattern structures as an etching mask to form third and fourth mask pattern structures, the third mask pattern structure formed on the first region and having a first upper surface. The fourth mask pattern structure formed on the second region and may have a second upper surface, a height of the second upper surface being greater than a height of the first upper surface. The etch target layer may be partially removed using the third and fourth mask pattern structures as an etching mask to form first and second patterns, the first pattern formed on the first region and having a third width, and the second pattern formed on the second region and having a fourth width. The fourth width may be greater than the third width.

[0023] In example embodiments, when the second mask pattern structure is formed, the third preliminary mask pattern may be removed. When the fourth mask pattern structure is formed, the second preliminary mask pattern may be removed.

[0024] In example embodiments, when the first mask pattern structure is formed, the first spacer may be removed. When the second mask pattern structure is formed, such that a first part of the second spacer may remain.

[0025] In example embodiments, when the first and spacer is formed, the first preliminary mask pattern may be formed on the second hard mask layer. A spacer layer may be formed on the second hard mask layer and the first preliminary mask pattern. A mask layer may be formed on the spacer layer on the second region. The spacer layer may be partially removed formed on the first region to form the first spacer. The forming the second spacer may include forming the second preliminary mask pattern on the second hard mask layer, forming the spacer layer on the (i) second hard mask layer and (ii) the second preliminary mask patterns, forming the mask layer on the spacer layer on the second region; removing the mask layer may; and partially removing the spacer layer on the second region to form the second spacer.

[0026] In the method of forming patterns of the semiconductor device in accordance with example embodiments, both of the first and second mask patterns having relatively small and large sizes, respectively, may be formed. There may be height difference between the first and second mask patterns, and thus process margin may be provided in the subsequently DPT process. Additionally, when the first and second mask patterns are formed, the amount of etching of the portion of the spacer layer on the first mask pattern may be controlled before and/or after removing the photoresist pattern, and thus the value of the height difference may be controlled.

[0027] According to an example embodiment, a method of forming patterns of a semiconductor device may include forming a height difference between a first preliminary mask pattern on a first region of a layer structure and a second preliminary mask pattern on a second region of the layer structure by etching at least a portion of the first preliminary mask pattern and at least a portion of the second preliminary mask pattern, the layer structure including a plurality of mask layers stacked on an etch target layer, the etch target layer on a substrate; and forming a first pattern structure on the first region and a second pattern structure on the second region by etching the plurality of mask layers, the etching of the plurality of mask layers controlled to maintain the height difference while forming of the first pattern structure and the second pattern structure.

[0028] According to an example embodiment, the first preliminary mask pattern may include a first sacrificial pattern on a second sacrificial pattern; and the forming the height difference may include, forming a spacer layer on an upper surface of the first sacrificial layer, on a sidewall of the first preliminary mask pattern, on an upper surface and on a sidewall of the second preliminary mask pattern, etching at least a portion of the spacer layer on the upper surface of the